LOCAL AREA

IP/MPLS/FIBER

1

U1

U2

U3

N7

S

S

PACKET

METRO AREA   BACKBONE

IP/MPLS
OC-12

IP/ATM/FIBER   N3
OC-192

U4

U5

IP/ATM/DSL

U6

U7

N1

S

S   S

CELL

IP/ATM
OC-12

6

10

IP/MPLS
OC-12

SONET MUX

7

OC-48

8

9

N5

R1

IP/ATM
OC-48

N6

IP/MPLS
OC-48

S

S

S   S

R4

R2

IP/MPLS/FIBER   R5
OC-192

R3

S

S   S

N4

N2

U8

S

S

U9

PACKET

IP/MPLS/ COAX

U10

FIG. 1
(PRIOR ART)

ROUTER
R1

TO/FROM
NETWORK N1

TO/FROM
NETWORK N2

ATM
LINE CARD   2

MPLS
LINE CARD   4

LINE CARD

11

ATM
LINE CARD   3

MPLS
LINE CARD   5

LINE CARD

TO/FROM
NETWORK N5

TO/FROM
NETWORK N6

FIG. 2
(PRIOR ART)

MULTISERVICE LINE
CARD 12

ATM AND
PACKET

ATM AND
PACKET

14

15

16

MUX/
DEMUX

17

ATM

18

PACKET

SWITCH
FABRIC

13

FIG. 3

ROUTER 100

CPU
106

115
PACKETS
ATM CELLS
AAL5 CELLS

116
PACKETS
ATM CELLS
AAL5 CELLS

131

LINE
CARD
101

107
SPI-4
SPI-4
108

SWITCH
FABRIC
105

109
SPI-4
SPI-4
110

LINE
CARD
103

117
PACKETS
ATM CELLS
AAL5 CELLS

118
PACKETS
ATM CELLS
AAL5 CELLS

PACKETS
ATM CELLS
AAL5 CELLS

PACKETS
ATM CELLS
AAL5 CELLS

136

LINE
CARD
102

111
SPI-4
SPI-4
112

113
SPI-4
SPI-4
114

LINE
CARD
104

137

PACKETS
ATM CELLS
AAL5 CELLS

PACKETS
ATM CELLS
AAL5 CELLS

FIG. 4

LINE CARD 101

131
FROM CPU

129
DRAM

127
SRAM

132
SERDES
121
133
123

119
OC-192
OPTICS

RX

F
R
A
M
E
R

124
CLASSIFICATION

125
MULTI-SERVICE SAR
(MS-SAR)

INGRESS MODE

SPI-4

107

115

SPI-4
134

SPI-4
135

SPI-4

LINE
SIDE

SWITCH
FABRIC
SIDE

116

120
OC-192
OPTICS

TX

122
SERDES

140

139

SPI-4
138

126
MULTI-SERVICE SAR
(MS-SAR)

EGRESS MODE

SPI-4

SPI-4

108

128
SRAM

130
DRAM

FIG. 5

SWITCH FABRIC	APPLICATION TYPE	INGRESS APPL TYPE	EGRESS APPL TYPE
CELL	ATM => ATM	0	8
	ATM => MPLS PACKET	1	9
	MPLS PACKET => ATM	2	10
	MPLS PACKET => MPLS PACKET	3	11
PACKET	ATM => PACKET	4	14
	PACKET => ATM	6	12
	AAL5 => PACKET	5	14
	PACKET => AAL5	6	13
	PACKET => PACKET	6	14

APPLICATION TYPES

FIG. 6

FIG. 7

FIG. 8

215
SSRAM
LUT
MEMORY #1

216
SSRAM
LUT
MEMORY #2

217
DDR-SDRAM
PAYLOAD
MEMORY
64-BYTE
BUFFERS

218
SSRAM
REASSEMBLY
MEMORY
STORES SWITCH
HEADERS

327
HEADER TABLE

FID   MPLS   SWITCH
         INFO   HEADER

MS-SAR
125, 200

201
INCOMING
SPI-4
INTERFACE

202
LOOKUP
ENGINE

203
SEGMENT-
ATION

204
MEMORY
MANAGER

205
REASSEMBLY
& HEADER
ADDING

206
OUTGOING
SPI-4
INTERFACE

326

198

16 BIT

317
64-BIT

318
64-BIT

319
128-BIT

324
128-BIT

325
64-BIT

211
CPU
INTERFACE

212

BID 321

ENQUEUE   DEQUEUE

320   323

213

208
DATA
BASE

207
PER FLOW
QUEUE

CPU
INTERFACE

214

209
TRAFFIC
SHAPER

210
OUTPUT
SCHEDULER

219
SSRAM
SHAPER
FID#1
MEMORY

220
SSRAM
SHAPER
FID#2
MEMORY

221
SSRAM
SHAPER
SLOT
MEMORY

222
SSRAM
FID NEXT
MEMORY

223
SSRAM
FID
MEMORY

224
SSRAM
PACKET
MEMORY

SSRAM
PFQ
STAT
MEMORY
225

SSRAM
PFQ
BID
MEMORY
FREE
BUFFER
QUEUE &
FLOW
QUEUES
226

SSRAM
PFQ
FID ENQ
MEMORY
TAIL
PTRS
227

SSRAM
PFQ
FID DEQ
MEMORY
HEAD
PTRS
228

FIG. 10

TYPE 3 FOR FLOW #1
TYPE 0 FOR FLOW #2

TYPE 11 FOR FLOW #1
TYPE 8 FOR FLOW #2

CPU
106

105

PACKET (FLOW #1)

ATM (FLOW #2)

115 101 135 121 125 107 103

119 123

INGRESS

CELL SWITCH FABRIC

110

EGRESS

141 144 143 142 118 200

PACKET (FLOW #1)

ATM (FLOW #2)

FIG. 9

MPLS PACKET RECEIVED
ONTO MS-SAR 300

END DELIMITER 304

START DELIMITER 302

DATA PAYLOAD 303

HEADER 301

FIG. 11

64-BYTE CHUNKS FROM SPI-4 INTERFACE

307 306 305

3 2 1

SIGNALS ADDED BY
SPI-4 INTERFACE AND
SENT TO LOOKUP
ENGINE

SOP=0
EOP=1

SOP=0
EOP=0

SOP=1
EOP=0

FIG. 12

TYPE 3 FOR FLOW #1
TYPE 0 FOR FLOW #2

MPLS
PACKET (FLOW
#1)

ATM
(FLOW #2)

201	202	203	204	205	206
SPI-4	LOOKUP ENGINE	SEGMENT-ATION ENGINE	MEMORY MANAGER	REASSEMBLY & HEADER ADDING	SPI-4

217
DDR-SDRAM
PAYLOAD MEMORY
64-BYTE BUFFERS

322

ENQUEUE   DEQUEUE

	207
DATA BASE	PER/FLOW QUEUE

208

209	210
TRAFFIC SHAPER	OUTPUT SCHEDULER

INGRESS MODE

FIG. 13

PORT TABLE IN LOOKUP BLOCK

64 LOGICAL INPUT PORTS

1		10000	0
45		10000	0

INPUT PORT NUMBER

NUMBER OF BYTES OF SWITCH HEADER (USED BY EGRESS)
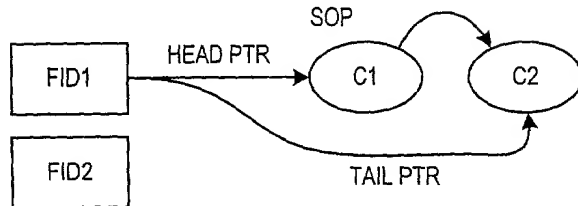
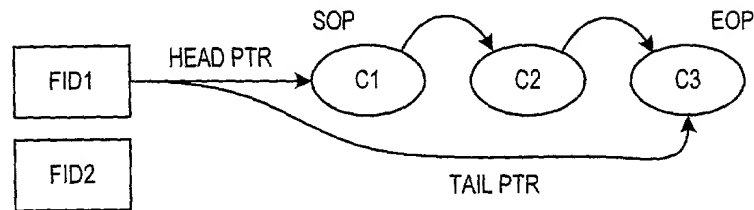TRAFFIC TYPE (USED BY INGRESS)

FIG. 14
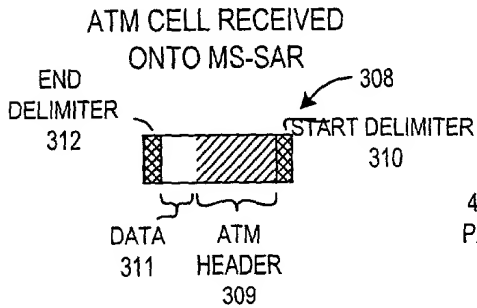
FIG. 15A

FIG. 15B

FIG. 15C

ATM CELL RECEIVED
ONTO MS-SAR

FIG. 20

56-BYTE CHUNK FROM
SPI-4 INTERFACE

FIG. 21

64-BYTE CHUNK FROM
SEGMENTATION BLOCK
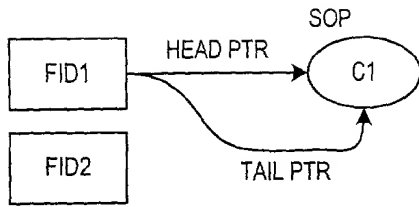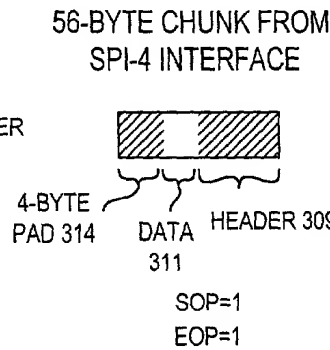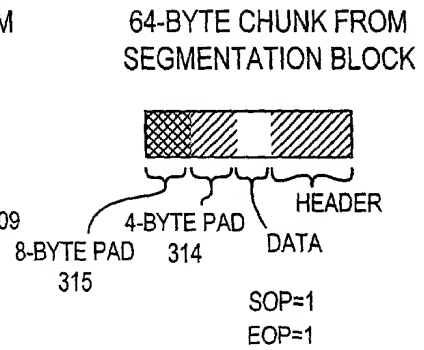
FIG. 22
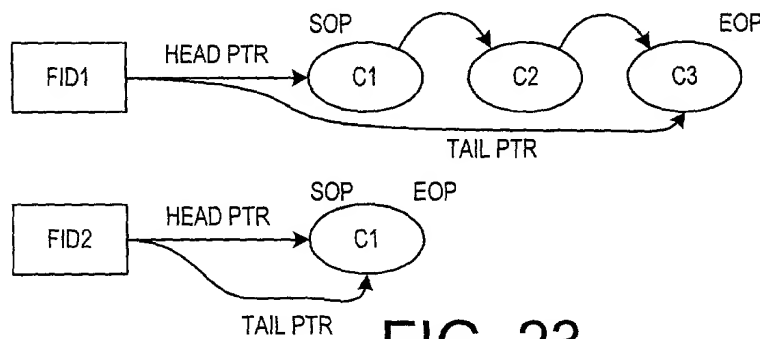
FIG. 23

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID HEAD	23	22:0	H	HEAD POINTER. FIRST BUFFER TO BE ENQUEUED, AND FIRST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.
HD EOP PKT	1	23	H	IF SET, THE HEAD BID IS THE EOP.
HD SOP PKT	1	23	H	IF SET, THE HEAD BID IS THE SOP.
HD EFCI	1	25	H	EFCI BIT.
CLP	1	26	H	CLP BIT. CAN BE MODIFIED BY DBS.
OAM	1	27	H	OAM BIT.
SPARE	1	28	H	
CLASS	3	31:29	H	CLASS OF FID.
FID TYPE	4	35:32	H	APPLICATION TYPE INDICATES THE PROCESSING THAT THE MS-SAR WILL TAKE ON THIS FLOW. WILL BE SENT TO MEMORY MANAGER. TYPE IS WRITTEN WITH THE HEAD POINTER.

FID DEQUEUE MEMORY LOCATION

FIG. 16

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID TAIL	23	22:0	H	TAIL POINTER. LAST BUFFER TO BE ENQUEUED, AND LAST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.
BID PRV PKT TAIL	23	45:23	H	BID OF PREVIOUS PACKET'S TAIL BID. SAVED ON EOP.
TTL	1	46	H	WHEN 1, DISCARD AND DEACTIVATE THE FID.
OUTPUT PORT#	7	53:47	S	OUTPUT PORT NUMBER THAT THE FID WILL BE TRANSMITTED ON.
Q SIZE	18	71:54	H	SIZE OF THE QUEUE IN BIDS. INCREMENTED ON ENQUEUE. DECREMENTED ON EVERY DEQUEUE OPERATION.

FIRST FID ENQUEUE MEMORY LOCATION

FIG. 17

NAME	NO BITS	RANGE	WR	DESCRIPTION
VALID	1	0	S	IF SET, THEN ENQUEUE. IF NOT, THEN SETUP CONNECTION COMMAND AS NEEDED BEFORE ENQUEUE STARTS.
SPARE	8	8:1		
DROP UNTIL SOP	1	9	H	DROP UNTIL THE NEXT SOP.
SEL DROP COUNT ER	1	10	H	SEL THE COUNT FOR DROPPING.
SPARE	2	12:11		
CURRENT TAIL PKT CELL CNT	11	23:13	H	REPRESENTS THE NUMBER OF CELLS IN THE TAIL PACKET THAT IS BEING ENQUEUED.
SPARE	2	25:24		
ENQ NOT DISCARD RED PKT COUNT	16	41:26	H	THE NUMBER OF NOT DISCARDED PACKETS THAT HAVE ARRIVED SINCE LAST RED DISCARD. IT IS RESET ON THE NEXT RED DISCARD.
SPARE	2	43:42		
AVG	18	61:44	H	THE AVE SIZE OF THE QUEUE.

SECOND FID ENQUEUE MEMORY LOCATION

FIG. 18

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID LINK	23	22:0	H	BID OF THE NEXT BUFFER IN FID QUEUE. ALSO CAN BE A BID LINKED ON THE FREE BUFFER QUEUE.
EOP PKT	1	23	H	END OF PACKET FOR THIS BID BID. EOP BELONGS TO THE BID LINK.
SOP PKT	1	24	H	START OF PACKET FOR THE CORRESPONDING BID. SOP BELONGS TO THE BID LINK.
EFCI	1	25	H	EFCI PASS THROUGH BIT.
OAM	1	26	H	OAM BIT.
CLP	1	27	H	CLP
SPARE	8	35:28		

BID MEMORY LOCATION

FIG. 19

PORT CALENDAR IN REASSEMBLY BLOCK

1	0	PID 1
		⋮

64 POSSIBLE OUTPUT PORT ENTRIES

JUMP BIT   VALID BIT   PORT ID

FIG. 24

64 BITS

| 1 0 0 0 0 0 0 0 • • • 0 0 0 |

PORT EMPTY REGISTER

FIG. 25

64 BITS

| 1 0 0 0 0 0 0 0 • • • 0 0 0 |

PORT FULL REGISTER

FIG. 26

DDR-SDRAM
PAYLOAD MEMORY
64-BYTE BUFFERS
217

TYPE 3 FOR FLOW #1
TYPE 0 FOR FLOW #2

201 SPI-4 → 202 LOOKUP ENGINE → 203 SEGMENT-ATION ENGINE → 204 MEMORY MANAGER → 205 REASSEMBLY & HEADER ADDING → 206 SPI-4 →

SWITCH CELLS TO SWITCH FABRIC

ENQUEUE   DEQUEUE

DATA BASE 208 ← → PER FLOW QUEUE 207

209 TRAFFIC SHAPER   210 OUTPUT SCHEDULER

INGRESS MODE

FIG. 27

SWITCH HEADER ADDED BY REASSEMBLY BLOCK

64-BYTES

SWITCH CELL #3

64-BYTES

SWITCH CELL #2

64-BYTES

SWITCH CELL #1

INDICATES EOP=1

AZANDA HEADER
(INCLUDES FID, TYPE, CLASS)

INDICATES SOP=1

FIG. 28

AZANDA HEADER
(INCLUDES FID, TYPE, CLASS)

SWITCH HEADER ADDED
BY REASSEMBLY BLOCK

64-BYTES

SWITCH CELL

FIG. 29

LOOKUP BLOCK LOCATES AZANDA HEADER,
DETERMINES APPLICATION TYPE

64-BYTES

SWITCH HEADER

SWITCH CELL #1

FIG. 31

DDR-SDRAM ⌐217

PAYLOAD
MEMORY

64-BYTE
BUFFERS

TYPE 11 FOR FLOW #1
TYPE 8 FOR FLOW #2

SWITCH CELLS FROM
SWITCH FABRIC

| 201 SPI-4 | 202 LOOKUP ENGINE | 203 SEGMENT-ATION ENGINE | 204 MEMORY MANAGER | 205 REASSEMBLY & HEADER ADDING | 206 SPI-4 |

ENQUEUE

DEQUEUE

207

DATA
BASE

PER FLOW
QUEUE

⌐209
TRAFFIC
SHAPER

⌐210
OUTPUT
SCHEDULER

EGRESS MODE

FIG. 30

EGRESS MODE
FIG. 32

FORMAT OF ONE FID ENTRY
IN HEADER TABLE
FIG. 33

64-BYTE CHUNKS FROM REASSEMBLY TO SPI-4

3	2	1

SOP=0
EOP=1

SOP=0
EOP=0

SOP=1
EOP=0

OUTPUT TO SPI-4 INTERFACE

FIG. 34

MPLS PACKET OUTPUT
TO FRAMER

END DELIMITER 303

START DELIMITER 301

DATA PAYLOAD 302

HEADER 300
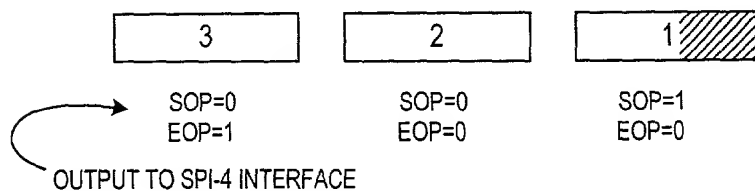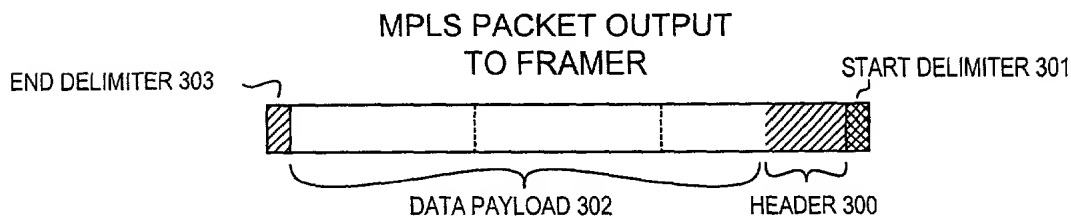
FIG. 35

56-BYTE CHUNK FROM
REASSEMBLY BLOCK

PAD
(4-BYTES)

DATA
(48-BYTES)

HEADER
(4-BYTES)

SOP=1
EOP=1

FIG. 36

ATM CELL AS OUTPUT
FROM SPI-4 INTERFACE

END DELIMITER

START DELIMITER

DATA
(48-BYTES)

HEADER
(4-BYTES)

FIG. 37

TYPE 5 FOR FLOW #1
TYPE 6 FOR FLOW #2

TYPE 14 FOR FLOW #1
TYPE 13 FOR FLOW #2

FIG. 38

| OUTPUT FROM INCOMING SPI-4 BLOCK 201 | OUTPUT FROM LOOKUP BLOCK 202 | OUTPUT FROM SEGMENTATION BLOCK 203 | OUTPUT FROM REASSEMBLY BLOCK 205 | FROM OUTGOING SPI-4 BLOCK 206 TO PACKET SWITCH FABRIC |

FLOW #1

INGRESS APPLICATION TYPE 5

FIG. 39

MPLS
PACKET

SWITCH PACKET

405 / 406 / 407 / 415 /

MPLS HDR	MPLS HDR		SWITCH HDR 8 OR 16 BYTES	SWITCH HDR 8 OR 16 BYTES
PACKET DATA 150 BYTES	PACKET DATA 150 BYTES	DATA 64 BYTES	MPLS HDR	MPLS HDR
			PACKET DATA 150 BYTES	PACKET DATA 150 BYTES

408

DATA
64 BYTES

409

DATA (26B) ⟵ 411
PAD ⟵ PAD 412
TRAILER ⟵ TRAILER WITH CRC (410)

416

416

PACKET BURST OUTPUT FROM INCOMING SPI-4 BLOCK 201	PACKET BURST OUTPUT FROM LOOKUP BLOCK 202	64-BYTE CELLS OUTPUT FROM SEGMENTATION BLOCK 203	OUTPUT FROM REASSEMBLY BLOCK 205	FROM OUTGOING SPI-4 BLOCK 206 TO PACKET SWITCH FABRIC

FLOW #2
INGRESS APPLICATION TYPE 6

FIG. 40

SWITCH
PACKET

MPLS
PACKET

413 / 418 / 432 /

SWITCH HDR 8 OR 16 BYTES			MPLS HDR	MPLS HDR
PACKET DATA 144 BYTES	PACKET DATA 144 BYTES	DATA 64 BYTES	PACKET DATA 144 BYTES	PACKET DATA 144 BYTES

419

DATA
64 BYTES

DATA
PAD
TRAILER

DATA 16 BYTES (421)
PAD
TRAILER WITH CRC (422)

414

417

420

434

433

434

PACKET BURST OUTPUT FROM INCOMING SPI-4 BLOCK 201	PACKET BURST OUTPUT FROM LOOKUP BLOCK 202	64-BYTE CELLS OUTPUT FROM SEGMENTATION BLOCK 203	OUTPUT FROM REASSEMBLY BLOCK 205	FROM OUTGOING SPI-4 BLOCK 206 TO LINE

FLOW #1
EGRESS APPLICATION TYPE 14

FIG. 41

SWITCH
PACKET

AAL5 CELLS

| SWITCH HDR
8 OR 16 BYTES | ← 415 | | | 423 | | | 425 | | | ATM HDR
4 BYTES | 435 | ATM HDR
4 BYTES | ← 436 |

SWITCH HDR
8 OR 16 BYTES   ← 415

MPLS HDR

MPLS HDR   423

ATM DATA #1
48 BYTES   425

ATM HDR
4 BYTES   435

ATM HDR
4 BYTES   ← 436

PACKET DATA 150
BYTES

PACKET DATA 150
BYTES

ATM DATA #1
48 BYTES

ATM DATA #1
48 BYTES

PAD
16 BYTES

PAD 4 BYTES

416

424

ATM HDR
4 BYTES

ATM HDR
4 BYTES   ← 437

ATM DATA #2
48 BYTES   426

ATM DATA #2
48 BYTES

ATM DATA #2
48 BYTES

PAD
16 BYTES

PAD 4 BYTES

ATM HDR
4 BYTES

ATM HDR
4 BYTES   ← 438

ATM DATA #3
48 BYTES   427

ATM DATA #3
48 BYTES

ATM DATA #3
48 BYTES

PAD
16 BYTES

PAD 4 BYTES

ATM HDR
4 BYTES

ATM HDR
4 BYTES   ← 439

ATM DATA #4   428

ATM DATA #4

ATM DATA #4

10 BYTES (429)

PAD 30 BYTES (431)

TRAILER 8 BYTES (430)

PAD
16 BYTES

PAD 4 BYTES

429
431
430

PACKET BURST
OUTPUT FROM
INCOMING SPI-4
BLOCK 201

PACKET BURST
OUTPUT FROM
LOOKUP BLOCK
202

64-BYTE CELLS
OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206 TO
LINE

FLOW #2
EGRESS APPLICATION TYPE 13

FIG. 42

AAL5
CELLS

SWITCH
CELLS

ATM HDR 4 BYTES	ATM HDR 4 BYTES		SWITCH HDR 8 OR 16 BYTES	SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #1 48 BYTES	AAL5 DATA #1 48 BYTES	AAL5 DATA #1 48 BYTES	AAL5 DATA #1 48 BYTES	AAL5 DATA #1 48 BYTES
	PAD 4 BYTES	PAD 16 BYTES	PAD 16 BYTES	PAD 16 BYTES

ATM HDR 4 BYTES	ATM HDR 4 BYTES		SWITCH HDR 8 OR 16 BYTES	SWITCH HDR 8 OR 16 BYTES
AAL5 DATA #2	AAL5 DATA #2	AAL5 DATA #2	AAL5 DATA #2	AAL5 DATA #2
PAD	PAD	PAD	PAD	PAD
TRAILER	TRAILER	TRAILER	TRAILER	TRAILER
	PAD 4 BYTES	PAD 16 BYTES	PAD 16 BYTES	PAD 16 BYTES

OUTPUT FROM INCOMING SPI-4 BLOCK 201   OUTPUT FROM LOOKUP BLOCK 202   OUTPUT FROM SEGMENTATION BLOCK 203   OUTPUT FROM REASSEMBLY BLOCK 205   FROM OUTGOING SPI-4 BLOCK 206

INGRESS APPLICATION TYPE 1

SWITCH
CELLS

MPLS
PACKET

SWITCH HDR 8 OR 16 BYTES	AAL5 DATA #1 48 BYTES	AAL5 DATA 48 BYTES	MPLS HDR 8 OR 16 BYTES	MPLS HDR 8 OR 16 BYTES
AAL5 DATA #1 48 BYTES			(AAL5 DATA #1 PLUS AAL5 DATA #2)	PACKET HDR
PAD 16 BYTES	PAD 16 BYTES	PAD 16 BYTES		PACKET DATA

SWITCH HDR 8 OR 16 BYTES	AAL5 DATA #2	AAL5 DATA #2
AAL5 DATA #2	PAD	PAD
PAD	TRAILER	TRAILER
TRAILER		
PAD 16 BYTES	PAD 16 BYTES	PAD 16 BYTES

OUTPUT FROM INCOMING SPI-4 BLOCK 201   OUTPUT FROM LOOKUP BLOCK 202   OUTPUT FROM SEGMENTATION BLOCK 203   OUTPUT FROM REASSEMBLY BLOCK 205   FROM OUTGOING SPI-4 BLOCK 206

EGRESS APPLICATION TYPE 9

FIG. 43

MPLS
PACKET

| MPLS HDR |
| PACKET DATA
72 BYTES |

| PACKET DATA
72 BYTES |

SWITCH
CELLS

| AAL5 DATA #1
48 BYTES |
| PAD 16 BYTES |

| SWITCH HDR
8 OR 16 BYTES |
| AAL5 DATA #1
48 BYTES |
| PAD 16 BYTES |

| SWITCH HDR
8 OR 16 BYTES |
| AAL5 DATA #1
48 BYTES |
| PAD 16 BYTES |

| AAL5 DATA #2 |
| PAD |
| TRAILER |
| PAD 16 BYTES |

| SWITCH HDR
8 OR 16 BYTES |
| AAL5 DATA #2 |
| PAD |
| TRAILER |
| PAD 16 BYTES |

| SWITCH HDR
8 OR 16 BYTES |
| AAL5 DATA #2 |
| PAD |
| TRAILER |
| PAD 16 BYTES |

OUTPUT FROM
INCOMING
SPI-4 BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

INGRESS APPLICATION TYPE 2

SWITCH
CELLS

| SWITCH HDR
8 OR 16 BYTES |
| AAL5 DATA #1
48 BYTES |
| PAD 16 BYTES |

| AAL5 DATA #1
48 BYTES |
| PAD 16 BYTES |

| AAL5 DATA
48 BYTES |
| PAD 16 BYTES |

AAL5
CELLS

| ATM HDR
4 BYTES |
| AAL5 DATA #1
48 BYTES |
| PAD 4 BYTES |

| ATM HDR
4 BYTES |
| AAL5 DATA #1
48 BYTES |

| SWITCH HDR
8 OR 16 BYTES |
| AAL5 DATA #2 |
| PAD |
| TRAILER |
| PAD 16 BYTES |

| AAL5 DATA #2 |
| PAD |
| TRAILER |
| PAD 16 BYTES |

| AAL5 DATA #2 |
| PAD |
| TRAILER |
| PAD 16 BYTES |

| ATM HDR
4 BYTES |
| AAL5 DATA #2 |
| PAD |
| TRAILER |
| PAD 4 BYTES |

| ATM HDR
4 BYTES |
| AAL5 DATA #2 |
| PAD |
| TRAILER |

OUTPUT FROM
INCOMING
SPI-4 BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

EGRESS APPLICATION TYPE 10

FIG. 44

ATM
CELL

SWITCH
PACKET

			SWITCH HDR 8 OR 16 BYTES	SWITCH HDR 8 OR 16 BYTES
ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES
ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES
	PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES
		PAD 8 BYTES	PAD 8 BYTES	PAD 8 BYTES

OUTPUT FROM
INCOMING
SPI-4 BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

INGRESS APPLICATION TYPE 4

SWITCH
PACKET

MPLS
PACKET

SWITCH HDR 8 OR 16 BYTES				
ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES	MPLS HDR	MPLS HDR
			ATM HDR 4 BYTES	ATM HDR 4 BYTES
ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES
PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES
PAD 8 BYTES	PAD 8 BYTES	PAD 8 BYTES		

OUTPUT FROM
INCOMING
SPI-4 BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

EGRESS APPLICATION TYPE 14

FIG. 45

MPLS PACKET
(ATM CELL
ENCAPSULATED)

SWITCH PACKET (ATM
CELL ENCAPSULATED)

| SWITCH HDR |
| 8 OR 16 BYTES |

MPLS HDR	MPLS HDR	MPLS HDR	MPLS HDR	MPLS HDR
ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES
ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES
	PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES
		PAD 8 BYTES		

| OUTPUT FROM INCOMING SPI-4 BLOCK 201 | OUTPUT FROM LOOKUP BLOCK 202 | OUTPUT FROM SEGMENTATION BLOCK 203 | OUTPUT FROM REASSEMBLY BLOCK 205 | FROM OUTGOING SPI-4 BLOCK 206 |

INGRESS APPLICATION TYPE 6

SWITCH PACKET (ATM
CELL ENCAPSULATED)

ATM
CELL

SWITCH HDR 8 OR 16 BYTES				
MPLS HDR				
ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES	ATM HDR 4 BYTES
ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES	ATM DATA 48 BYTES
PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES	PAD 4 BYTES	
		PAD 8 BYTES		

| OUTPUT FROM INCOMING SPI-4 BLOCK 201 | OUTPUT FROM LOOKUP BLOCK 202 | OUTPUT FROM SEGMENTATION BLOCK 203 | OUTPUT FROM REASSEMBLY BLOCK 205 | FROM OUTGOING SPI-4 BLOCK 206 |

EGRESS APPLICATION TYPE 12
(ATM DE-ENCAPSULATION)

FIG. 46

AZA-003/2001-P003

MPLS
PACKET

SWITCH PACKET

SWITCH HDR
8 OR 16 BYTES

SWITCH HDR
8 OR 16 BYTES

MPLS HDR	MPLS HDR	DATA 64 BYTES	MPLS HDR	MPLS HDR
PACKET DATA 160 BYTES	PACKET DATA 160 BYTES	DATA 64 BYTES	PACKET DATA 160 BYTES	PACKET DATA 160 BYTES

DATA (36B) — DATA 440

PAD (20B) — PAD 442

TRAILER (8B) — TRAILER WITH CRC (441)

OUTPUT FROM
INCOMING SPI-4
BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

64-BYTE CELLS
OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

INGRESS APPLICATION TYPE 6

SWITCH
PACKET

MPLS
PACKET

SWITCH HDR
8 OR 16 BYTES

MPLS HDR	MPLS HDR	DATA 64 BYTES	MPLS HDR	MPLS HDR
PACKET DATA 160 BYTES	PACKET DATA 160 BYTES	DATA 64 BYTES	PACKET DATA 160 BYTES	PACKET DATA 160 BYTES

DATA

PAD

TRAILER — TRAILER WITH CRC (443)

OUTPUT FROM
INCOMING
SPI-4 BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

EGRESS APPLICATION TYPE 14

FIG. 47

FIG. 48

PACKET OUT OF DISTRIBUTION CHIP

END DELIMITER 526

START DELIMITER 525

PACKET DATA 523

PACKET HEADER 524

SEQUENCE NUMBER 527

FIG. 49

FID1

HEAD PTR

P5 → P6 ⤏ P8 → P9

TAIL PTR

PACKET QUEUE

FIG. 50

FID1

HEAD PTR

P6 → P7 → P8 → P9 → P10

TAIL PTR

PACKET QUEUE

FIG. 51

8 CLOCKS

INFO #1

INFO #2

529

ONE MEMORY CHIP

2 CLOCKS

INFO #1

530

2 CLOCKS

INFO #2

531

TWO MEMORY CHIPS

FIG. 52

FIG. 53

INCOMING SPI-4 INTERFACE BLOCK

FIG. 54

INPUT CONTROL BLOCK

FIG. 55
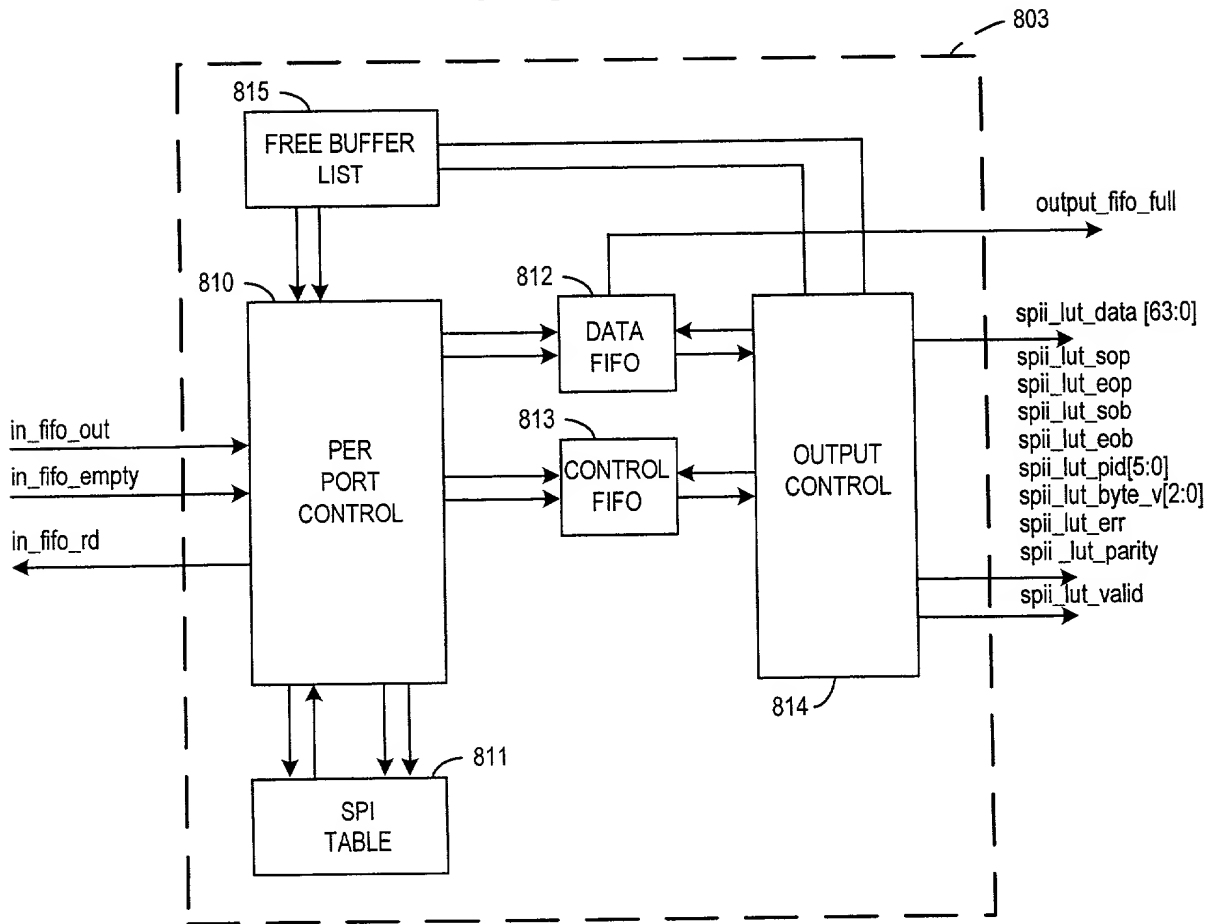
OUTPUT CONTROL BLOCK

FIG. 56
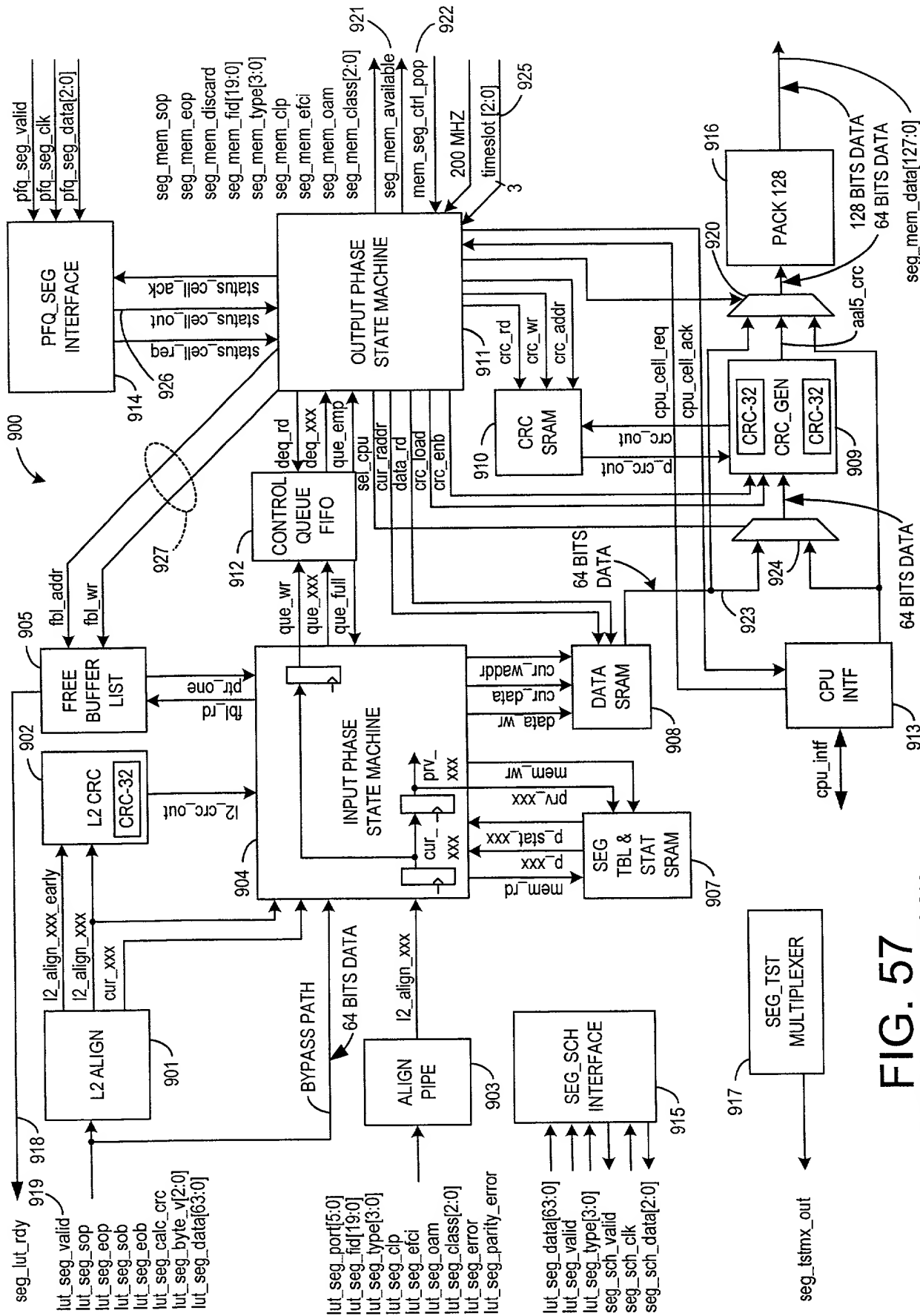
FIG. 57
SEGMENTATION BLOCK

FIG. 58

MEMORY MANAGER BLOCK

FIG. 58A

FIG. 58B

MEMORY MANAGER BLOCK 1000

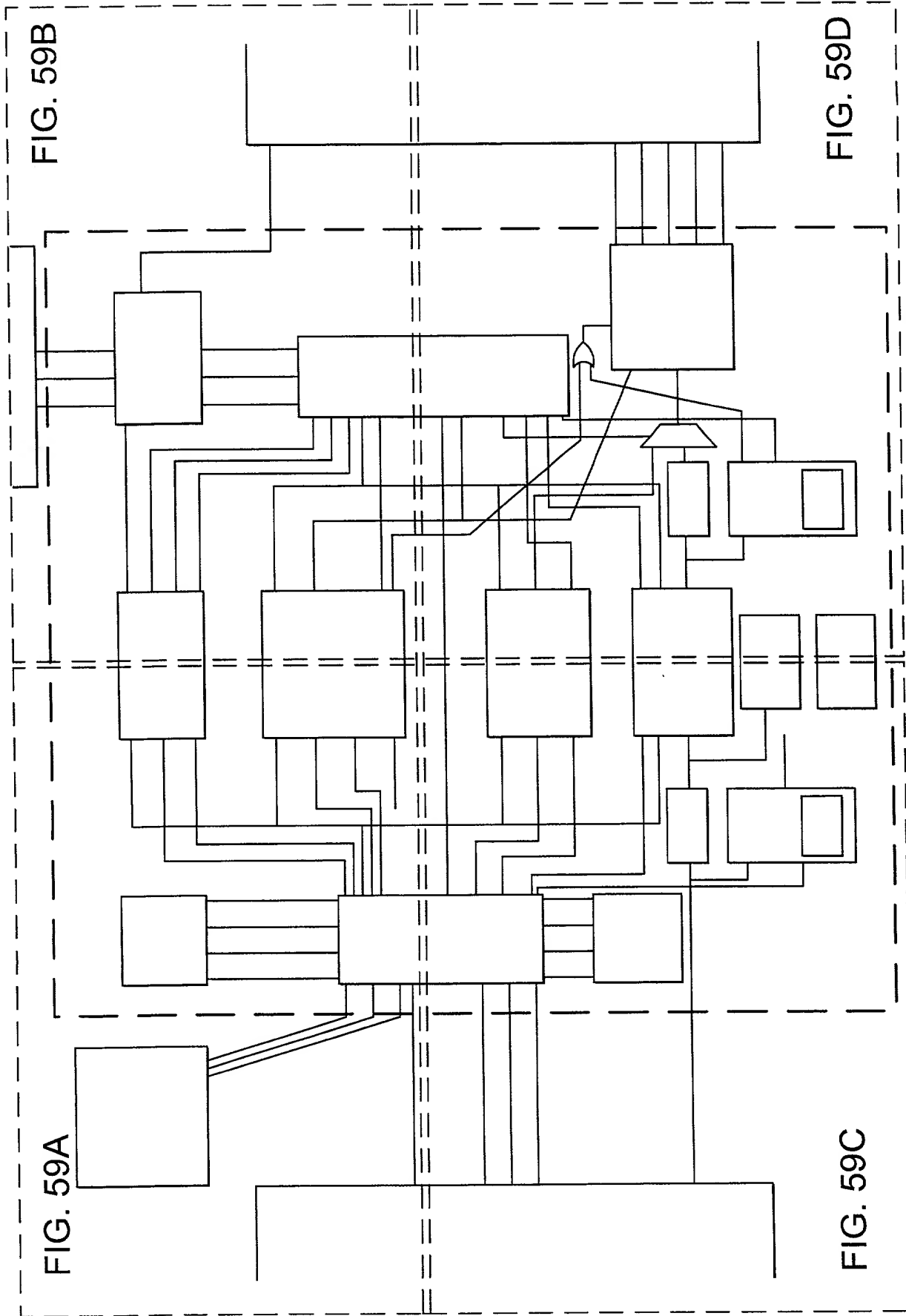SRAM ADAPTER 1002

REASSEMBLY BLOCK 205

1008

CELL COMPOSITION

DATA

BID/CNTL

MEMORY CONTROLLER

PAYLOAD MEMORY 217

1007

CPU INTERFACE 1003

BID

CNTL

DEQUEUE CONTROL 1005

PFQ INTERFACE

1006

PER FLOW QUEUE BLOCK 207

BID

DATA

ENQUEUE CONTROL 1004

CELL DEPOSITORY MANAGER 1001

SEGMENTATION BLOCK 203
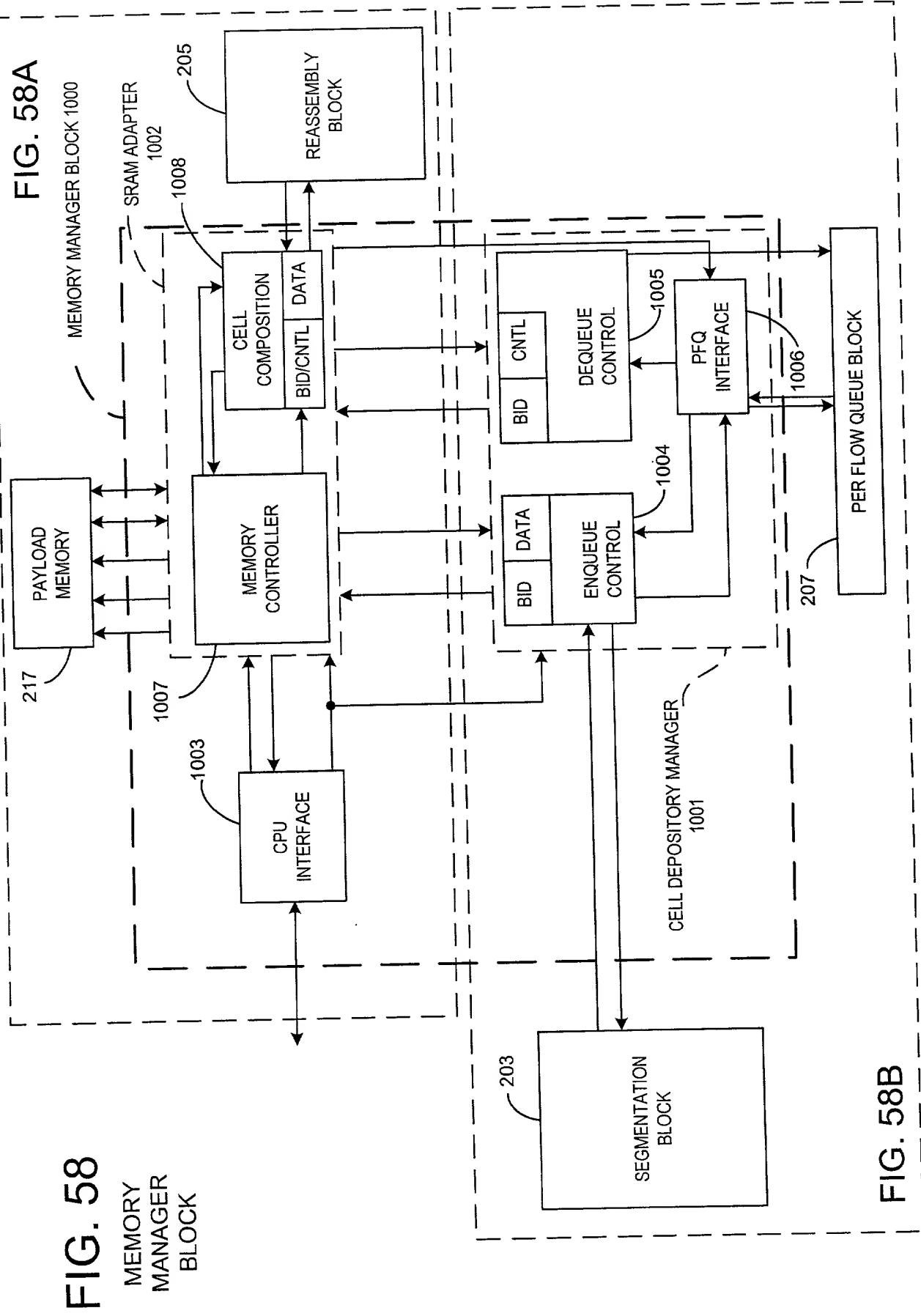
FIG. 58A
MEMORY MANAGER BLOCK

FIG. 58B

MEMORY MANAGER BLOCK
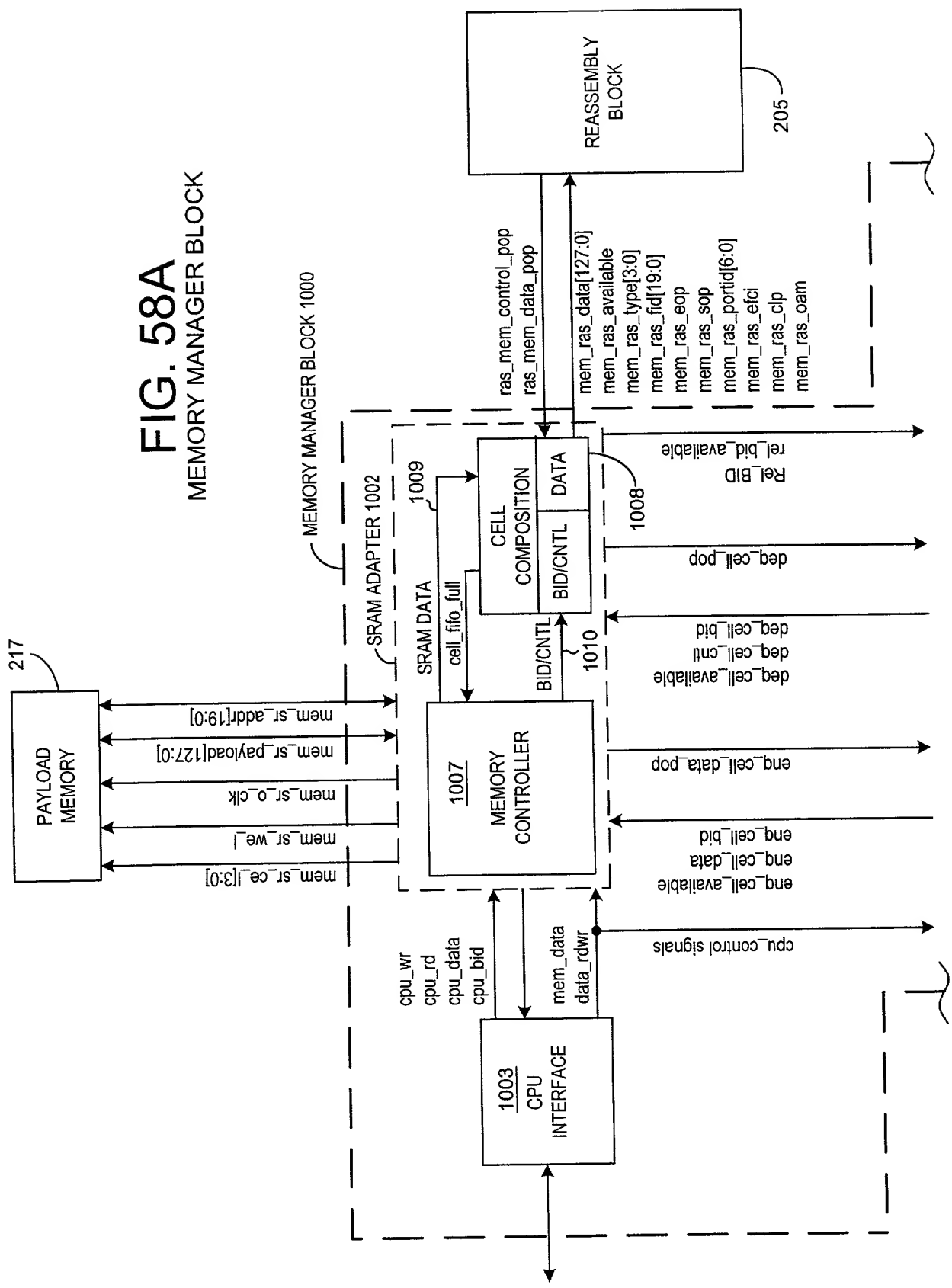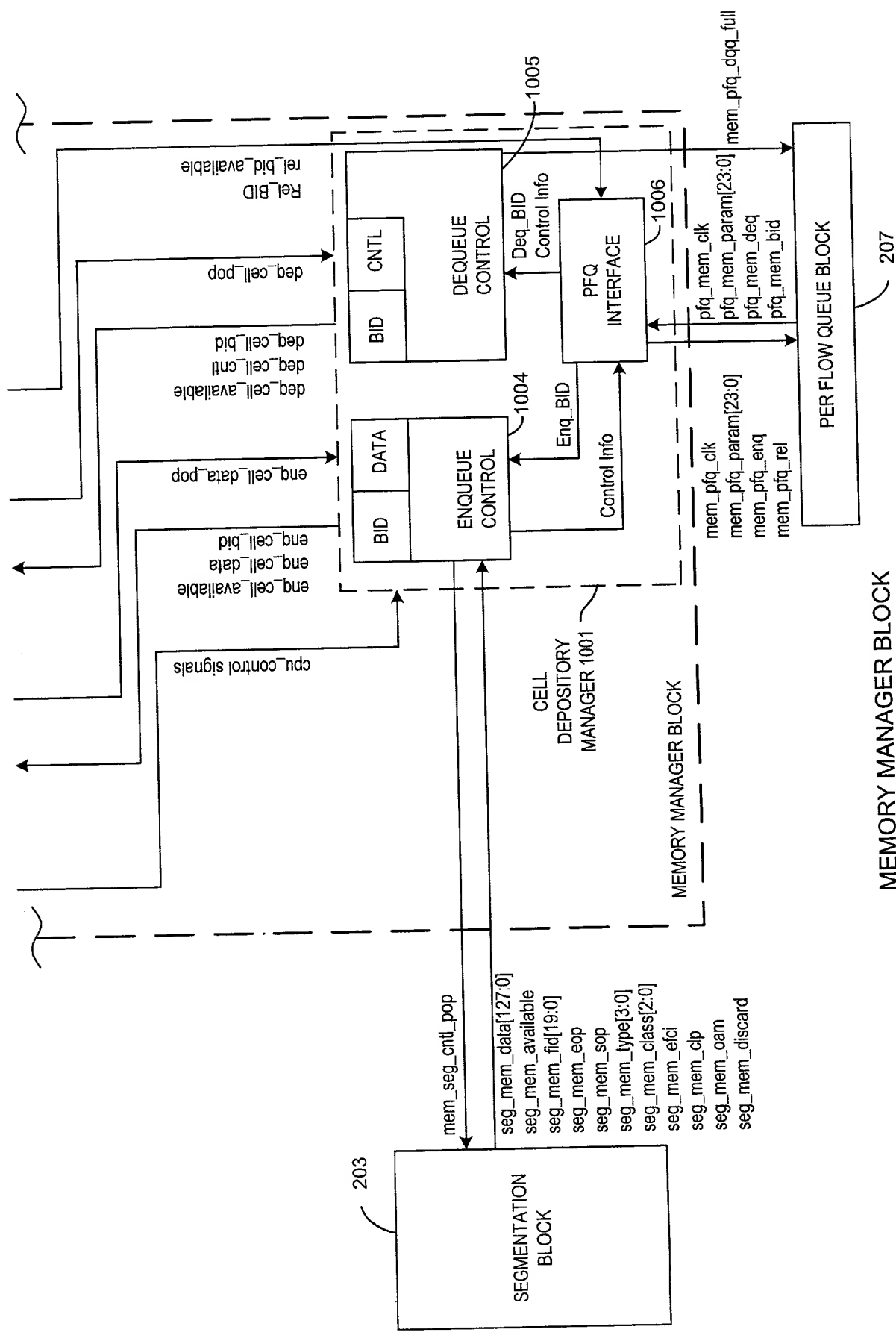
FIG. 59B

FIG. 59D

FIG. 59A

FIG. 59C

FIG. 59

REASSEMBLY BLOCK

FIG. 59A

REASSEMBLY BLOCK 1100

OUTPUT PORT QUEUE 64x24 BITS 1104

ADDR

wr

enq_data

pid

CONTROL SRAM 128x32 BITS 1105

ADDR

rd/wr

ctrl_data

ptr[6:0]

aal5_crc_ok

rd/wr

1126

FREE BUFFER LIST 128x7 BITS 1102

request 1120

ptr[6:0] 1121

release 1131

ptr[6:0] 1130

ENQUEUE STATE MACHINE 1101

(CHANGES TAIL)

EXTERNAL REASSEMBLY MEMORY 4Mx36 BITS 218

ADDR

1125

hdr_data [35:0]

fid[19:0]

rd

MEMORY MANAGER BLOCK 204

mem_ras_sop
mem_ras_eop
mem_ras_fid[19:0]
mem_ras_pid[6:0]
mem_ras_type[3:0]
mem_ras_clp
mem_ras_efci
mem_ras_oam
mem_ras_class[2:0]

FIG. 59B

OUTGOING SPI-4 INTERFACE BLOCK 206

port_status[7:0]

DATA BASE BLOCK 208

PORT FULL REGISTER 1141

PORT CALENDAR 64x8 BITS 1109

clk

sync

out_pid[6:0] 1128

pid_valid

request 1127

ras_dbs_status[8:0]

PORT EMPTY REGISTER 1140

DEQUEUE STATE MACHINE 1108 (CHANGES HEAD)

empty_status[63:0]

rd/wr

deq_data

ADDR 1104

OUTPUT PORT QUEUE 64x24 BITS

rd

next_rd_ptr[6:0], next_hdr_wd[1:0], sop, eop, pend, type[3:0], L2LEN cell length[5:0], L2HDR[4:0], bad

rd_ptr[6:0]

aal5_crc_ok 1137

ADDR

CONTROL SRAM 128x32 BITS 1105

FIG. 59C

FIG. 59D
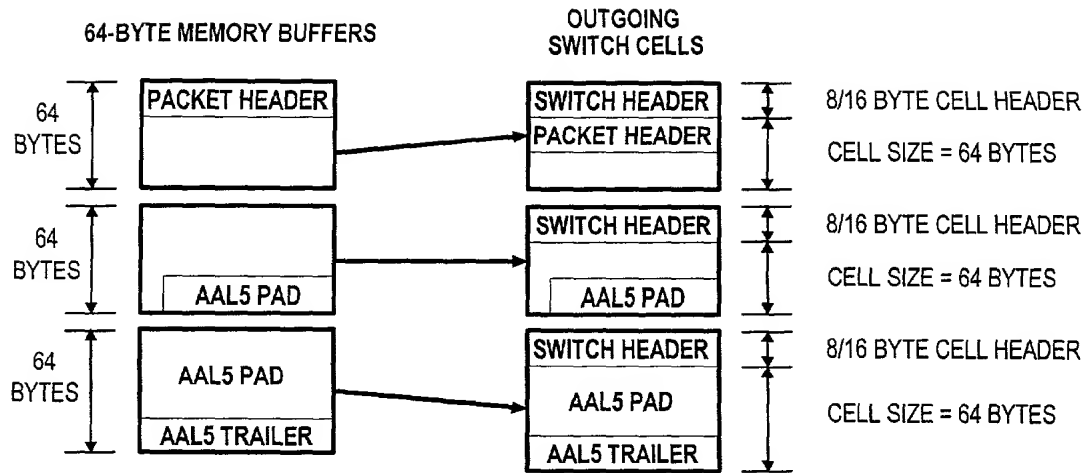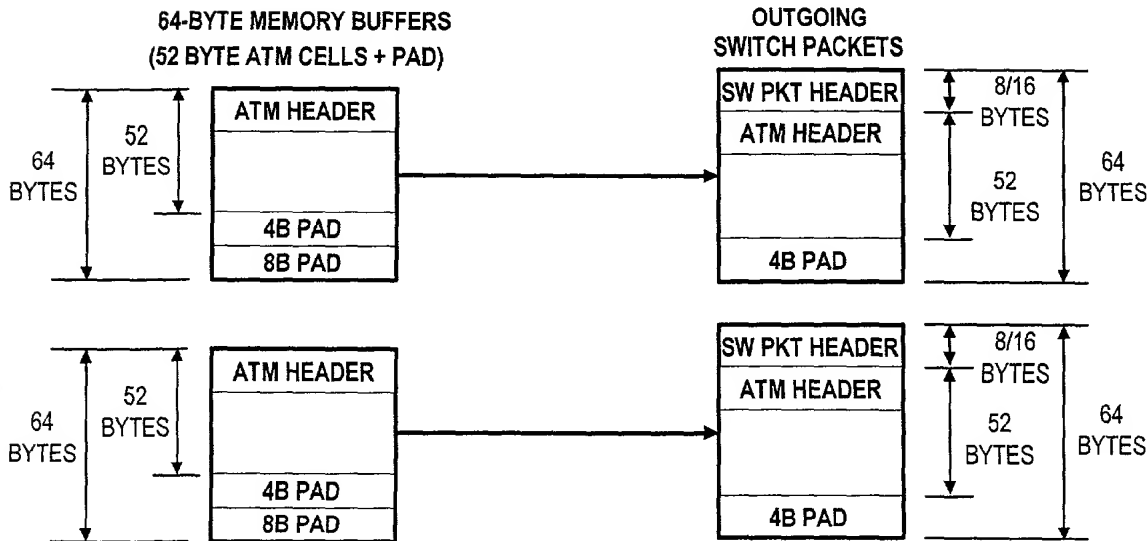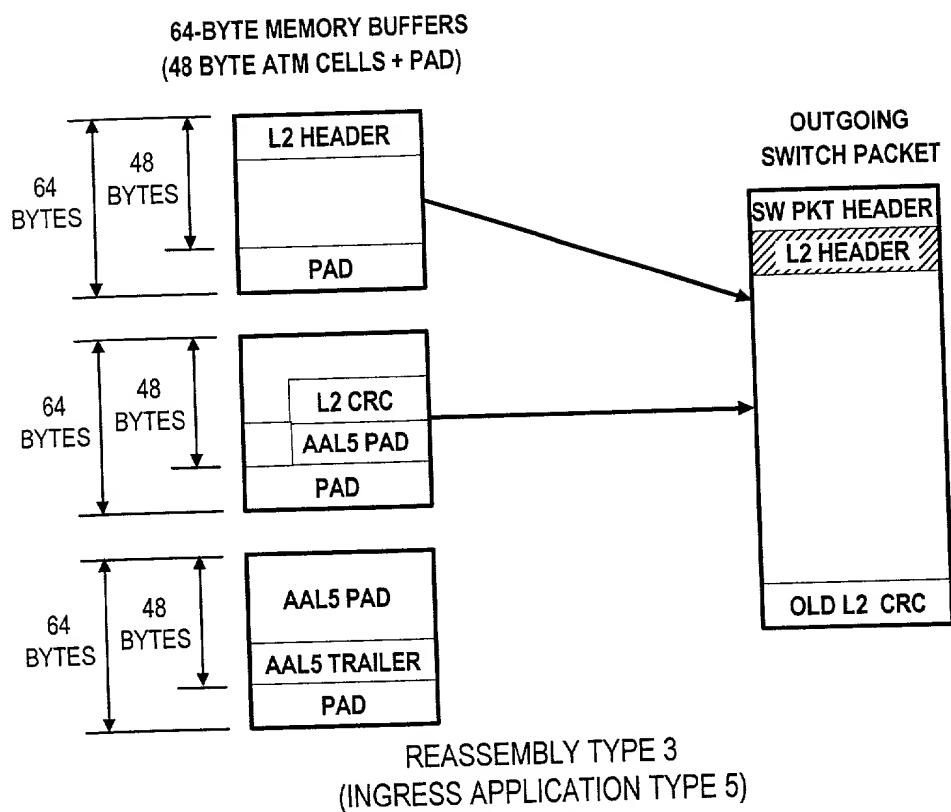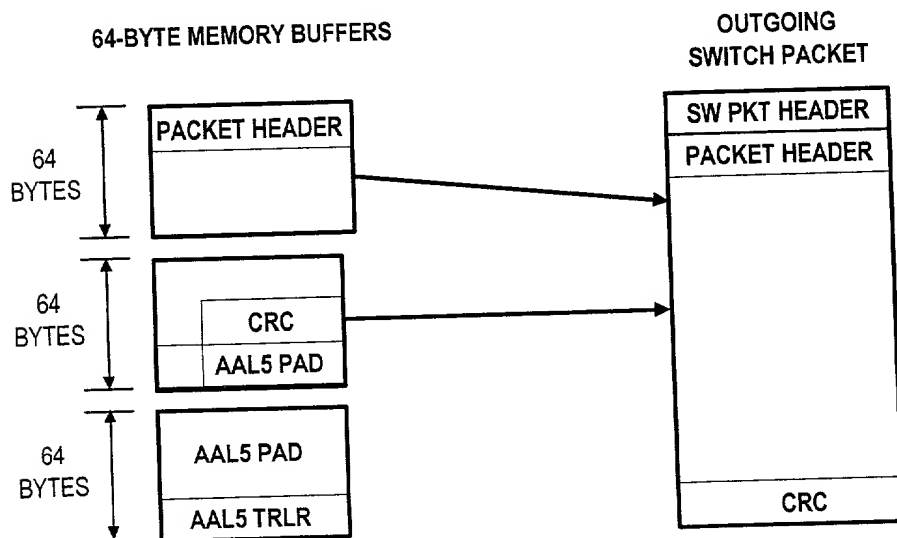
REASSEMBLY TYPE 1
(INGRESS APPLICATION TYPE 0)

FIG. 60A
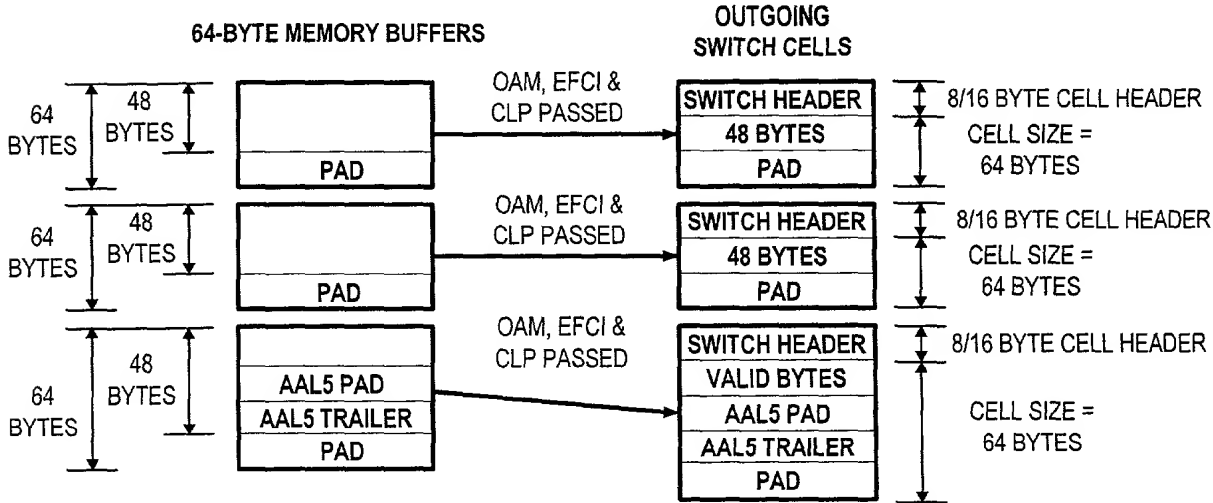
REASSEMBLY TYPE 1
(INGRESS APPLICATION TYPE 1)

FIG. 60B

64-BYTE MEMORY BUFFERS

OUTGOING
SWITCH CELLS

64 BYTES — PACKET HEADER → SWITCH HEADER / PACKET HEADER — 8/16 BYTE CELL HEADER / CELL SIZE = 64 BYTES

64 BYTES — AAL5 PAD → SWITCH HEADER / AAL5 PAD — 8/16 BYTE CELL HEADER / CELL SIZE = 64 BYTES

64 BYTES — AAL5 PAD / AAL5 TRAILER → SWITCH HEADER / AAL5 PAD / AAL5 TRAILER — 8/16 BYTE CELL HEADER / CELL SIZE = 64 BYTES

REASSEMBLY TYPE 1
(INGRESS APPLICATION TYPE 3)

FIG. 60C

64-BYTE MEMORY BUFFERS
(52 BYTE ATM CELLS + PAD)

OUTGOING
SWITCH PACKETS

64 BYTES / 52 BYTES — ATM HEADER / 4B PAD / 8B PAD → SW PKT HEADER / ATM HEADER / 4B PAD — 8/16 BYTES / 52 BYTES / 64 BYTES

64 BYTES / 52 BYTES — ATM HEADER / 4B PAD / 8B PAD → SW PKT HEADER / ATM HEADER / 4B PAD — 8/16 BYTES / 52 BYTES / 64 BYTES

REASSEMBLY TYPE 2
(INGRESS APPLICATION TYPE 4)

FIG. 60D

64-BYTE MEMORY BUFFERS
(48 BYTE ATM CELLS + PAD)

OUTGOING
SWITCH PACKET

64 BYTES — 48 BYTES

L2 HEADER
PAD

64 BYTES — 48 BYTES

L2 CRC
AAL5 PAD
PAD

64 BYTES — 48 BYTES

AAL5 PAD
AAL5 TRAILER
PAD

SW PKT HEADER
L2 HEADER
OLD L2 CRC

REASSEMBLY TYPE 3
(INGRESS APPLICATION TYPE 5)

FIG. 60E

64-BYTE MEMORY BUFFERS

OUTGOING
SWITCH PACKET

64 BYTES

PACKET HEADER

64 BYTES

CRC
AAL5 PAD

64 BYTES

AAL5 PAD
AAL5 TRLR

SW PKT HEADER
PACKET HEADER
CRC

REASSEMBLY TYPE 4
(INGRESS APPLICATION TYPE 6)

FIG. 60F

64-BYTE MEMORY BUFFERS
(ATM CELLS + PAD)

OUTGOING
ATM CELLS
NEW VPI/VCI

64
BYTES

52
BYTES

ATM HEADER

PAD

REPLACE CLP

ATM HEADER

52
BYTES

64
BYTES

52
BYTES

ATM HEADER

PAD

REPLACE CLP

ATM HEADER

52
BYTES

REASSEMBLY TYPE 5
(EGRESS APPLICATION TYPES 8 AND 12)

FIG. 60G

64-BYTE MEMORY BUFFERS
(48 BYTES ATM CELLS + PAD)

OUTGOING
PACKET

64
BYTES

48
BYTES

PACKET HEADER

PAD

MPLS LABEL

PACKET HEADER

64
BYTES

48
BYTES

AAL5 PAD

PAD

64
BYTES

48
BYTES

AAL5 PAD

AAL5 TRAILER

PAD

REASSEMBLY TYPE 6
(EGRESS APPLICATION TYPE 9)

FIG. 60H

64-BYTE MEMORY BUFFERS
(48 BYTE ATM CELLS + PAD)

OUTGOING
AAL-5 CELLS

REPLACE OAM, CLP & EFCI

64 BYTES | 48 BYTES

PAD

ATM HEADER

52 BYTES

REPLACE OAM, CLP & EFCI

64 BYTES | 48 BYTES

AAL5 PAD
PAD

ATM HEADER

AAL5 PAD

52 BYTES

REPLACE OAM, CLP & EFCI

64 BYTES | 48 BYTES

AAL5 PAD
AAL5 TRAILER
PAD

ATM HEADER
AAL5 PAD
AAL5 TRAILER

52 BYTES
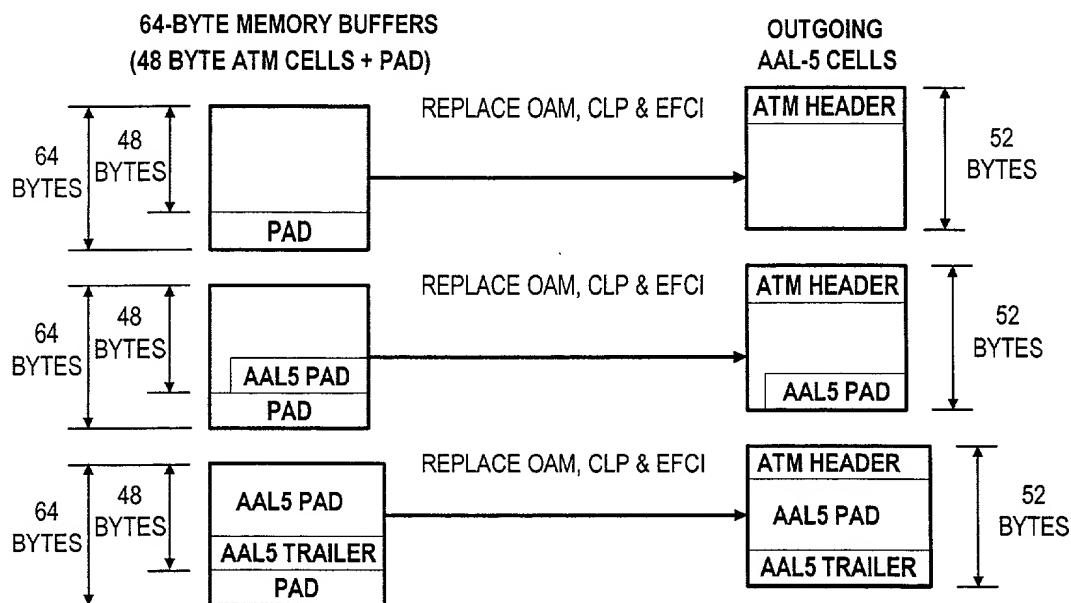
REASSEMBLY TYPE 7
(INGRESS APPLICATION TYPES 10 AND 13)

FIG. 60I

64-BYTE MEMORY BUFFERS

OUTGOING
PACKET

64 BYTES

PACKET HEADER

MPLS LABEL
PACKET HEADER

64 BYTES

64 BYTES

CRC
AAL5 PAD
AAL5 TRAILER

CRC
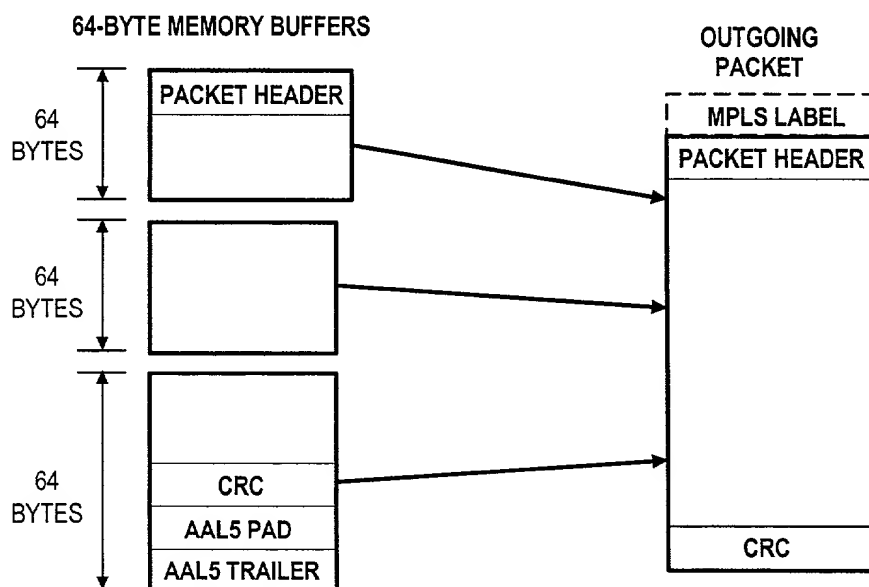
REASSEMBLY TYPE 8
(INGRESS APPLICATION TYPES 11 AND 14)

FIG. 60J

FIG. 61B

FIG. 61A

205

Figure 61

200 MHz | 400 MHz

SPIO_FF

1209

64-16 UNPACK ENGINE 1207

TX STATE MACHINE 1206

DATA PARITY GENERATION 1208

DATA FIFO DUAL PORT 4X83BIT 1205

RX STATE MACHINE 1203

PER PORT FIFO DUAL PORT 256X83BIT 1204

REASSEMBLY BLOCK

CONFIG REG 9X16 1202

SYNC

PORT CALENDAR DUAL PORT 64X7 BIT

PORT CALENDAR STATE MACHINE 1201

PARITY CHECK/ FRAME DETECT

PACK

STATUS FIFO 4X16

CPU INTERFACE

g_sync

REASSEMBLY BLOCK

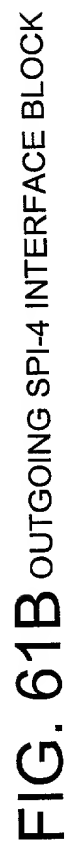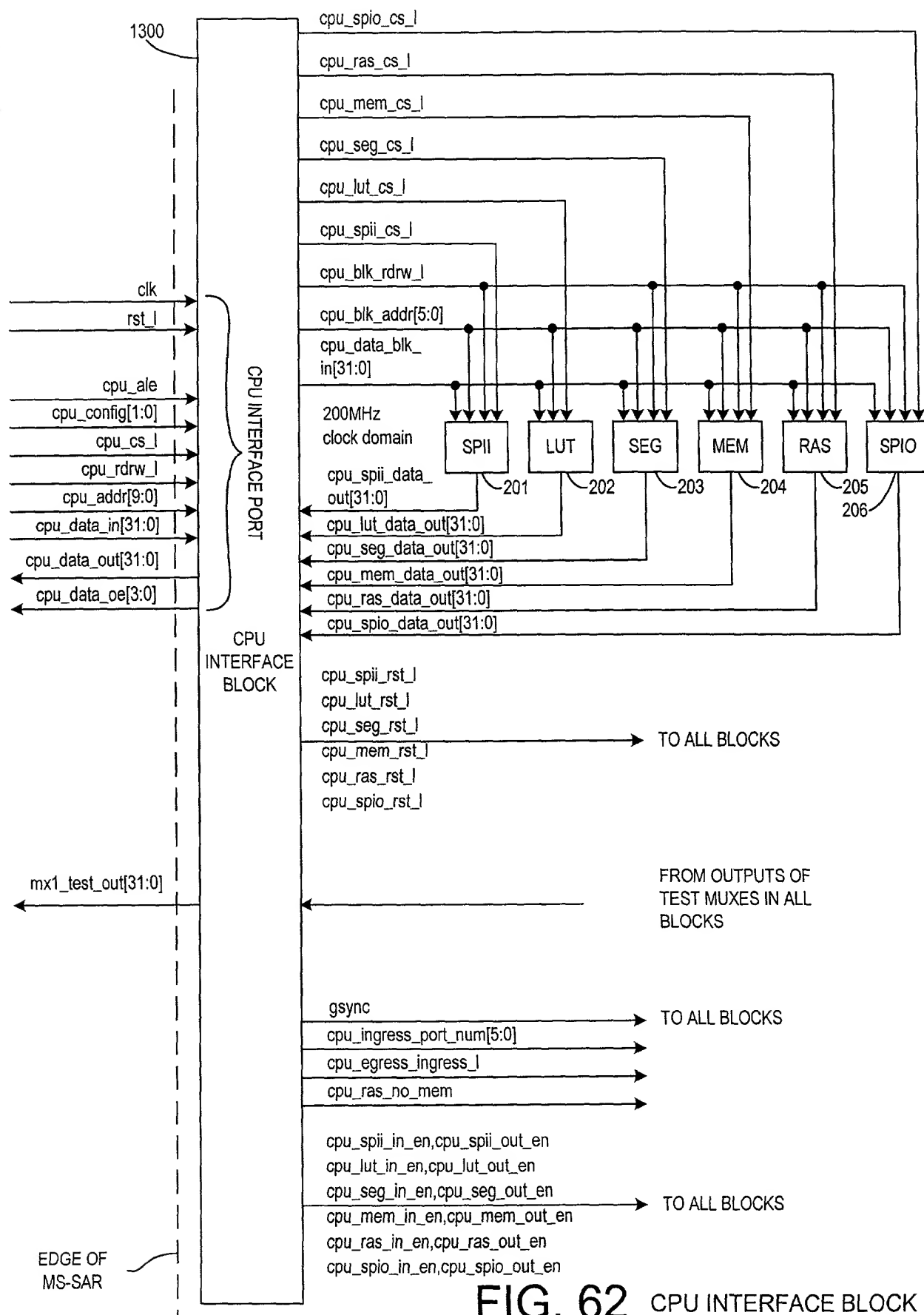FIG. 61 OUTGOING SPI-4 INTERFACE BLOCK

FIG. 61A

OUTGOING SPI-4 INTERFACE BLOCK

FIG. 61B OUTGOING SPI-4 INTERFACE BLOCK

FIG. 62 CPU INTERFACE BLOCK